Optimizing Total Power of Many-core Processors Considering Voltage Scaling Limit and Process Variations

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Outline

- Introduction
  - Supply Voltage and Power Scaling
    - Supply Voltage Scaling of Many-Core Processors
    - Power Scaling of Many-Core Processors
  - Impacts of Within-Die (WID) Spatial Process Variations
    - Global Clocking
    - Frequency–Island Clocking
  - Conclusions

Multicore processors

- Parallel Processing
  - Improved throughput of computing systems w/ more cores
  - Throughput is limited by power+thermal constraints w/ all cores running
- Challenges: How do we
  - Determine # of cores for best performance-power efficiency?
  - Exploit process variations for multicore processors?

[Image: GPU which has many cores [2]]

Process variations

- Types of Process variations
  - Die-to-Die (D2D) Variations
  - Within-Die (WID) Variations

[Image: Wafer Scale
  Courtesy: K. Bowman from Intel
  The corresponding NVM Fmax and Pmax map
  C2C frequency and leakage power variations due to spatial correlated WID variations become considerable.

Supply Voltage Scaling

- Supply voltage scaling of many-core processors
  - Throughput w/ certain # of cores at max \( V_{D\text{D}} \) (thus \( F_{\text{max}} \)) = Throughput w/ more cores at lower \( V_{D\text{D}} \) (thus \( F_{\text{max}} \))
  - Potential throughput increase by many cores and lower \( V_{D\text{D}} \) can reduce power.

[Image: Supply Voltage Scaling 1]

Supply Voltage Scaling 2

- Supply voltage scaling of many-core processors
  - \( M \cdot T_{\text{cycle}}(V_{D\text{D}}) = M \cdot ((1-F) + F/N) \cdot T_{\text{cycle}}(V) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M )</td>
<td>Number of operations</td>
</tr>
<tr>
<td>( T_{\text{cycle}} )</td>
<td>Cycle time of a processor at supply voltage</td>
</tr>
<tr>
<td>( V_{D\text{D}} )</td>
<td>Nominal supply voltage of base core processor</td>
</tr>
<tr>
<td>( F )</td>
<td>Fraction of operations parallelizable w/o overhead</td>
</tr>
<tr>
<td>( N )</td>
<td>Relative number of cores</td>
</tr>
<tr>
<td>( V )</td>
<td>Scaled supply voltage of the core cores</td>
</tr>
</tbody>
</table>

[Image: Supply Voltage Scaling 2]
### Dynamic Power Analysis

- **Dynamic power scaling**
  - Dynamic power of a base many-core processor
    \[ P_{\text{dyn,base}} = C_{\text{eff}} \cdot V_{\text{DD}} \cdot F_{\text{max}}(V_{\text{DD}}) \]
  - Dynamic power of N x more cores than the base processor
    \[ P_{\text{dyn,N}} = \left( (1-F) + (N-1) \cdot K + F \cdot N \right) \cdot C_{\text{eff}} \cdot F_{\text{max}}(V_{\text{DD}}) \]
    \[ = k(F,K, N) \cdot f(V) \cdot (V/V_{\text{DD}})^2 \cdot P_{\text{dyn,base}} \]

- **Leakage power scaling**
  - Leakage power of a base many-core processor
    \[ P_{\text{leak,base}} = I_{\text{leak}}(V_{\text{DD}}) \cdot V_{\text{DD}} \]
  - Leakage power of N x more cores than the base processor
    \[ P_{\text{leak,N}} = N \cdot I_{\text{leak}}(V_{\text{DD}}) \cdot V_{\text{DD}} \]

**Symbols and Units**
- \( P \): Power
- \( C_{\text{eff}} \): Effective total switching capacitance
- \( V_{\text{DD}} \): Nominal voltage of the base core
- \( k(F,K, N) \): Dynamic power of idle cores
- \( f(V) \): Frequency scaling factor at V
- \( V/V_{\text{DD}} \): Leakage scaling factor at V
- \( I_{\text{leak}} \): Total Leakage current of the base processor
- \( I_{\text{leak}}(V) \): Leakage current of the base processor

### Leakage Power Analysis

- **Leakage power scaling**
  - In nanoscale technology, leakage power is significant fraction of total power consumption.
  - Leakage power of a base many-core processor
    \[ P_{\text{leak,base}} = I_{\text{leak}}(V_{\text{DD}}) \cdot V_{\text{DD}} \]
  - Leakage power of N x more cores than the base processor
    \[ P_{\text{leak,N}} = N \cdot I_{\text{leak}}(V_{\text{DD}}) \cdot V_{\text{DD}} \]

**Symbols and Units**
- \( I_{\text{leak}} \): Total Leakage current of the base processor
- \( V_{\text{DD}} \): Nominal voltage of the base core

### Total Power Analysis

- **Total power scaling**
  - The total power of a base many-core processor is the sum of dynamic and leakage power.
    \[ P_{\text{tot,base}} = P_{\text{dyn,base}} + P_{\text{leak,base}} \]
  - The total power of N x more cores than the base processor is the sum of dynamic and leakage power.
    \[ P_{\text{tot,N}} = P_{\text{dyn,N}} + P_{\text{leak,N}} \]
    \[ = k(F,K, N) \cdot f(V) \cdot (V/V_{\text{DD}})^2 \cdot P_{\text{dyn,base}} + N \cdot (I(V) \cdot (V/V_{\text{DD}}) \cdot LF) \]

**Symbols and Units**
- \( P_{\text{tot}} \): Total power of a base core
- \( LF \): Ratio between \( P_{\text{leak}} \) and \( P_{\text{tot}} \) (\( P_{\text{leak}}/P_{\text{tot}} \))
Impacts of WID Variations – GC

- Global Clocking
  - Limits $F_{\text{max}}$ of a many-core processor to that of slowest core.
  - Previous $P_{\text{leak}}$ equation still can be used to estimate $P_{\text{leak}}$.
  - Estimation of $P_{\text{leak}}$ have to account for each core’s leakage variations as follows.
    $P_{\text{leak}} = \sum (f_i \cdot V_{\text{DD}}^2 \cdot P_{\text{leak, base}})$

- Frequency–Island Clocking
  - FI clocking is more performance and power efficient than GC because each core can run at its own fastest frequency.
  - Previous GC $P_{\text{leak}}$ equation can be used to estimate $P_{\text{leak}}$.
  - The equation for supply voltage scaling have to be modified as follows.
    $V_{\text{DD}} = \frac{V_{\text{DD, base}}}{(1-F) + F \cdot \sum f_i}$
  - Estimation of $P_{\text{leak}}$ also have to account for an independent clock frequency per core.
    $P_{\text{leak}} = (1-F) \cdot \sum f_i \cdot K \cdot V_{\text{DD}}^2 \cdot P_{\text{leak, base}}$
  - The fastest one among the chosen active cores always offers the optimal total power for processing the totally sequential portion of workload.

Impact of WID Variations – FI

- Frequency–Island Clocking
  - FI clocking is more performance and power efficient than GC and allows for faster cores.
  - On average, FI clocking offers 7% lower total power consumption than GC.

Experimental Methodology

- HSPICE simulations
  - 32nm PTM HP and LP model
  - Frequency / Leakage scaling factor
    - A range of $V_{\text{DD}} : 0.55 - 1.05(V)$
    - Complex gates for measuring $V_{\text{DD}}$

- $V_{\text{DD}}$ and $L_{\text{leak}}$ WID spatial and D2D variation map

Conclusions

- Optimal number of active cores to minimize total power consumption of many-core processors.
  - 2x more active cores at lower voltage offer more than 50% of total power reduction at the same throughput with a base core.
- Extended power analysis considering WID C2C frequency and leakage variations
  - 2x more active cores at lower voltage is the optimal choice.
- FI clocking provides lower power consumption than GC since it can exploit C2C variations. Also the fastest one in active cores for sequential portion of application led to the lowest power consumption.
Introduction

- Process variations
  - Manufactured dies exhibit a large spread of transistor delay and leakage power across die and within each die.
  - Die-to-die (D2D) variations affect all transistors on a die equally. Within-die (WID) variations induce different characteristics across each die.
  - As individual core size becomes smaller, core-to-core (C2C) frequency and leakage power variations due to spatial correlated WID variations will become considerable.

Supply Voltage and Power Scaling

- Supply voltage scaling of many-core processors
  - Throughput w/ a certain # of cores at max $V_{DD}$ (thus $F_{max}$)
  - = Throughput w/ more cores at lower $V_{DD}$ (thus $F_{real}$)
  - Potential throughput increase by many cores and lower $V_{DD}$ can reduce power.